



THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant: Foster, Donald Craig  
Assignee: Amkor Technology, Inc.  
Title: Stackable Lead Frame Package Using Exposed Internal Lead Traces  
Serial No.: 09/829,341 Filed: April 9, 2001  
Examiner: D. Zarneke Group Art Unit: 2812  
Docket No.: M-9950 US

Newport Beach, California  
August 21, 2001

BOX NO-FEE AMENDMENT  
COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D. C. 20231

### PRELIMINARY AMENDMENT

Dear Sir:

Please enter the following preliminary amendments in the above-identified application prior to the examination.

#### IN THE CLAIMS

The following is a clean version of the entire set of pending claims. In accordance with 37 C.F.R. § 1.121(c)(I)(iii), Attachment A provides marked up versions of the claims containing the newly introduced changes. Claims 15-32 have been canceled, and Claims 33-50 have been added.

1. A semiconductor die package, comprising:

conductive outer leads having first ends extending outside the package and second ends extending toward the interior of the package;

conductive inner leads having first ends extending to and electrically accessible through a first surface of the package; and

a first die electrically connected to the inner and outer leads.

2. The package of Claim 1, wherein the first ends of the outer leads do not extend beyond the first ends of the inner leads.

3. The package of Claim 1, wherein the first ends of the outer leads extend beyond the first ends of the inner leads.

4. The package of Claim 1, wherein the first surface is a bottom surface.

5. The package of Claim 4, further comprising a printed circuit board electrically coupled to the outer and inner leads.

6. The package of Claim 4, wherein the first ends of the inner leads are approximately co-planar with the first ends of the outer leads.

7. The package of Claim 4, wherein the first die is positioned above the inner leads.

8. The package of Claim 1, wherein the first surface is an upper surface.

9. The package of Claim 8, wherein the first die is positioned between the outer leads and the inner leads.

10. The package of Claim 8, further comprising a second semiconductor die package coupled to the first die, wherein the second semiconductor die package comprises a second die and outer leads coupled to the second die.

11. The package of Claim 10, wherein the outer leads of the second die are electrically coupled to the inner leads of the first die.

12. The package of Claim 11, wherein the second die package is positioned over the first die.

13. The package of Claim 1, wherein the inner leads further comprise an interior portion electrically accessible through the first surface, and wherein the die is further electrically coupled to the interior portion.

14. The package of Claim 13, wherein the interior portion and the first ends of the inner leads and the first ends of the outer leads are electrically coupled to a printed circuit board.

33. (New) The package of Claim 1, wherein the conductive inner leads are formed from an internal paddle area.

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34. (New) The package of Claim 33, further comprising means for securing and electrically isolating the conductive inner leads.

35. (New) The package of Claim 33, wherein the first die is attached to the internal paddle area.

36. (New) The package of Claim 33, wherein the first ends of the inner leads are closer to the die than the first ends of the outer leads.

37. (New) The package of Claim 33, wherein the first ends of the inner leads extend beyond the second ends of the outer leads.

38. (New) The package of Claim 33, wherein the first ends of the inner leads do not extend beyond the second ends of the outer leads.

39. (New) A semiconductor die package, comprising:

a lead frame having external leads;

internal leads electrically isolated from the external leads and secured to the lead frame;

means for securing and electrically isolating the internal leads from each other;

a die electrically coupled to the external leads and the internal leads; and

means for encapsulating the die and portions of the internal and external leads,

wherein the ends of the internal leads are exposed through a surface of the means for encapsulating.

40. (New) The package of Claim 39, wherein the internal leads are formed from an internal paddle area.

41. (New) The package of Claim 40, wherein the ends of the internal leads are exposed through a bottom surface of the means for encapsulating.

42. (New) The package of Claim 40, wherein the ends of the internal leads are exposed through a top surface of the means for encapsulating.

43. (New) The package of Claim 42, further comprising a second die package overlying the die package and electrically coupled to the internal leads of the die contained within the die package.

44. (New) The package of Claim 40, wherein the ends of the internal leads are bent towards the surface of the means for coupling.

45. (New) The package of Claim 40, wherein the external leads have first ends extending outside the means for encapsulating and second ends extending toward the die, and wherein the second ends of the external leads extend beyond the ends of the internal leads.

46. (New) A semiconductor die package, comprising:

a die;

an enclosure protecting the die;

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external leads each having a first and a second end, wherein the first ends extend beyond the enclosure and the second ends are electrically coupled to the die; and

internal leads having at least first ends exposed through the enclosure, wherein the die is electrically coupled to the internal leads, and wherein the internal leads are electrically isolated from the external leads.

47. (New) The package of Claim 46, wherein the first ends of the internal and external leads are approximately co-planar.

48. (New) The package of Claim 46, where the first ends of the internal and external leads are located on opposite sides of the enclosure.

49. (New) The package of Claim 48, further comprising a second die located over the die and electrically coupled to the first ends of the internal leads.

50. (New) The package of Claim 46, wherein the first ends of the internal leads and the second ends of the external leads are interleaved.

#### REMARKS

Claims 1-32 are pending in the present application. Claims 15-32 have been canceled in the accompanying Response to Restriction Requirement, and Claims 33-50 have been added. No new matter is added.

If the Examiner has any questions regarding the application, the Examiner is invited to

call the undersigned Attorney at (949) 718-5200.

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Respectfully submitted,



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